FIG. 1

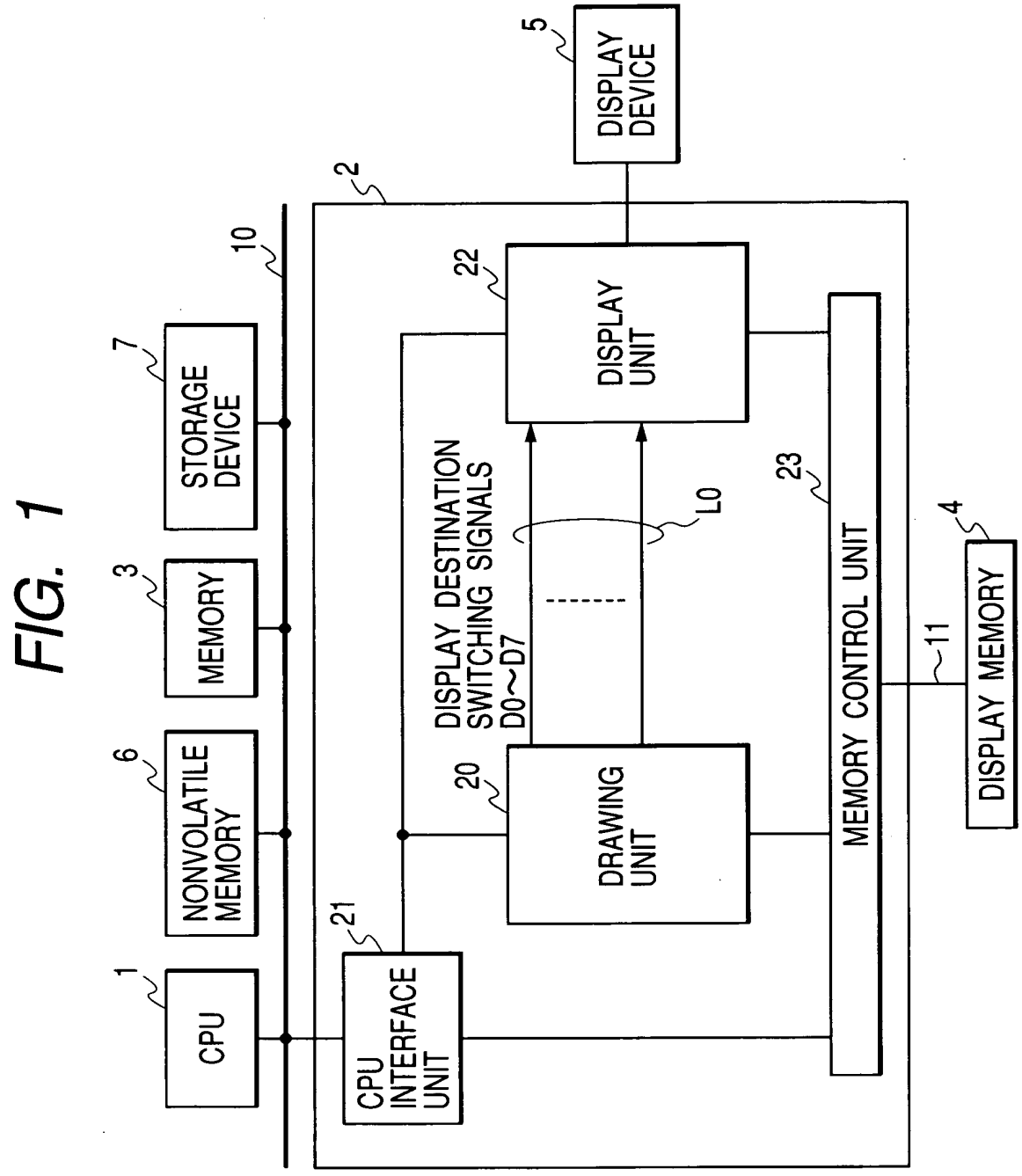

CPU
1
NONVOLATILE MEMORY
6
MEMORY
3
STORAGE DEVICE
7
10
2
CPU INTERFACE UNIT
21
DRAWING UNIT
20
DISPLAY UNIT
22
DISPLAY DESTINATION SWITCHING SIGNALS D0~D7
L0
MEMORY CONTROL UNIT
23
11
DISPLAY MEMORY
4
DISPLAY DEVICE
5

FIG. 2

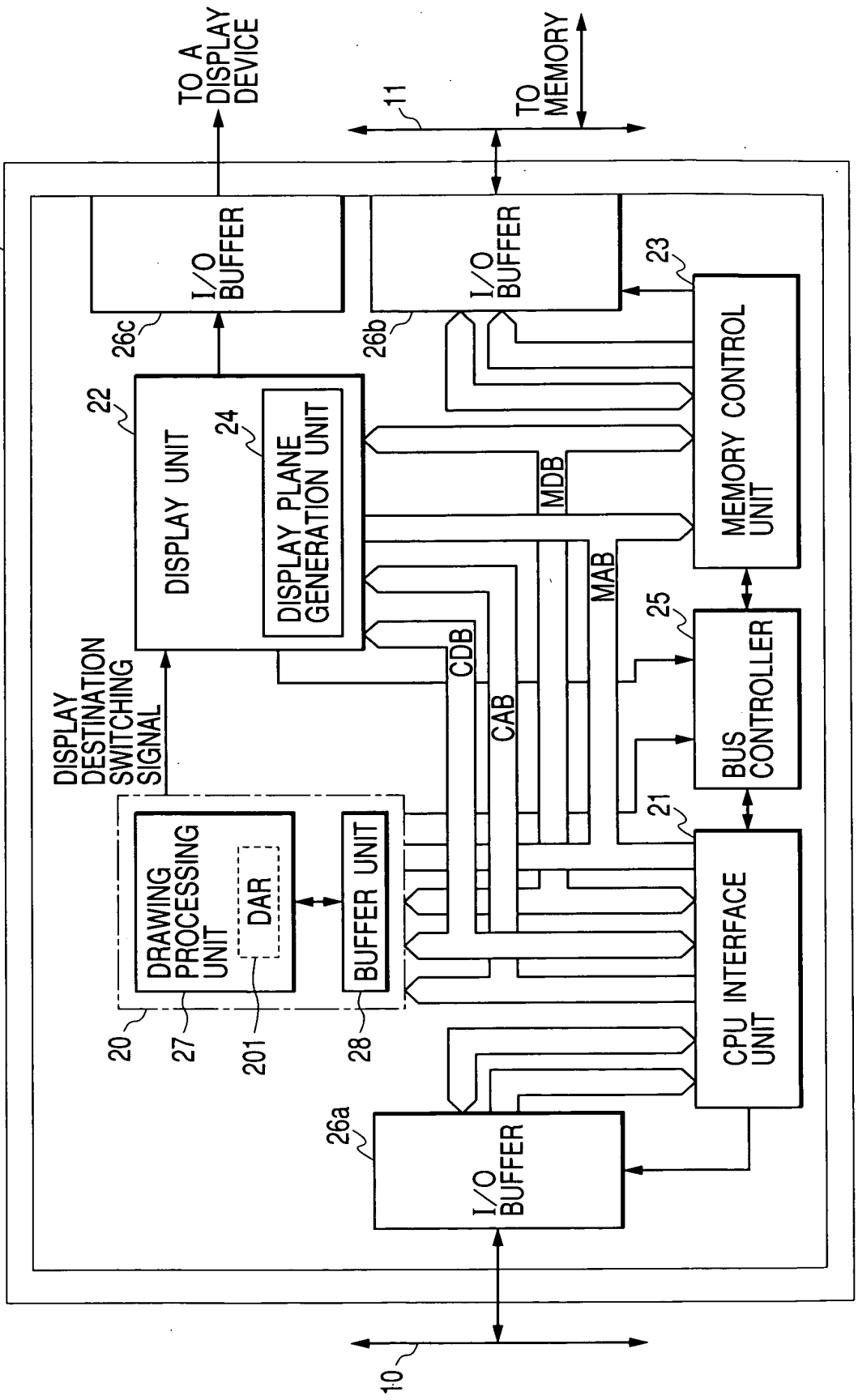

TO A DISPLAY DEVICE
11
TO MEMORY
2
I/O BUFFER
26c
I/O BUFFER
26b
23
22
DISPLAY UNIT
24
DISPLAY PLANE GENERATION UNIT
MDB
MEMORY CONTROL UNIT
MAB
25
CDB
CAB
BUS CONTROLLER
DISPLAY DESTINATION SWITCHING SIGNAL
21
DRAWING PROCESSING UNIT
DAR
BUFFER UNIT
CPU INTERFACE UNIT
20
27
201
28
26a
I/O BUFFER
10

FIG. 3

DRAWING ATTRIBUTE REGISTER

201

0	AUTOMATIC SWITCHING MODE ENABLE D0
1	AUTOMATIC SWITCHING MODE ENABLE D1
2	AUTOMATIC SWITCHING MODE ENABLE D2
3	AUTOMATIC SWITCHING MODE ENABLE D3
4	AUTOMATIC SWITCHING MODE ENABLE D4
5	AUTOMATIC SWITCHING MODE ENABLE D5
6	AUTOMATIC SWITCHING MODE ENABLE D6
7	AUTOMATIC SWITCHING MODE ENABLE D7
8	
⋮	⋮
26	
27	
28	
29	
30	
31	

FIG. 4

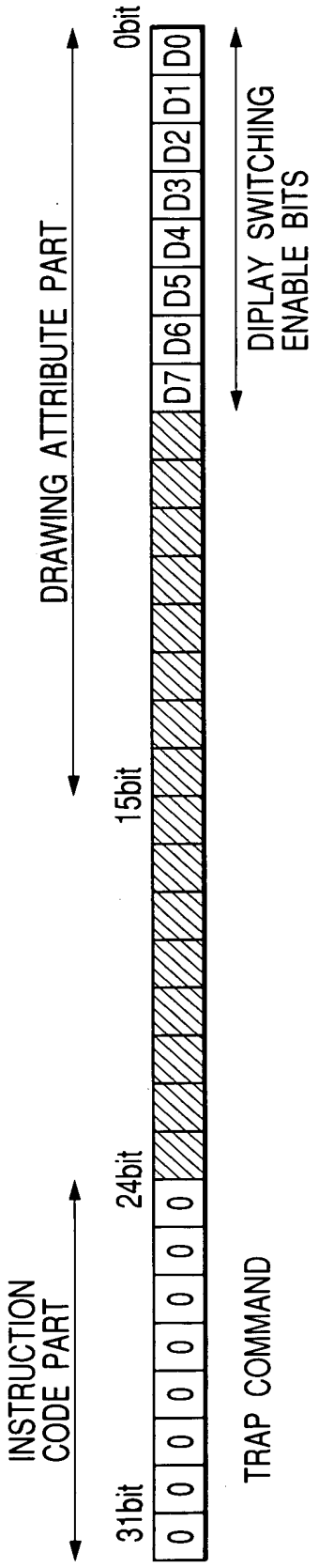

0bit
15bit
24bit
31bit
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 0 0 0
DRAWING ATTRIBUTE PART
DIPLAY SWITCHING ENABLE BITS
INSTRUCTION CODE PART
TRAP COMMAND

FIG. 5

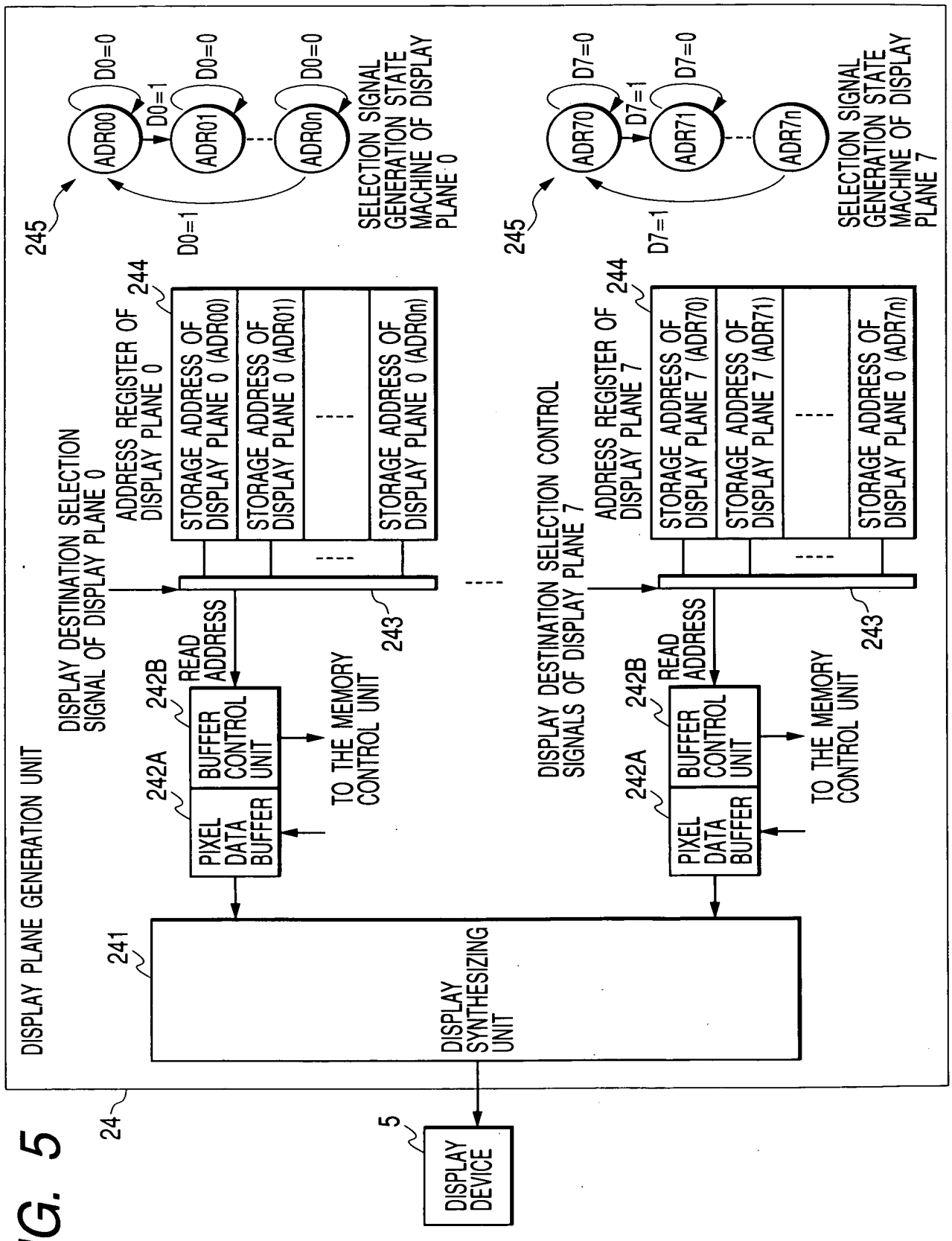

DISPLAY PLANE GENERATION UNIT
24
DISPLAY DESTINATION SELECTION SIGNAL OF DISPLAY PLANE 0
DISPLAY DESTINATION SELECTION CONTROL SIGNALS OF DISPLAY PLANE 7
ADDRESS REGISTER OF DISPLAY PLANE 0
ADDRESS REGISTER OF DISPLAY PLANE 7
244
STORAGE ADDRESS OF DISPLAY PLANE 0 (ADR00)
STORAGE ADDRESS OF DISPLAY PLANE 0 (ADR01)
STORAGE ADDRESS OF DISPLAY PLANE 0 (ADR0n)
STORAGE ADDRESS OF DISPLAY PLANE 7 (ADR70)
STORAGE ADDRESS OF DISPLAY PLANE 7 (ADR71)
STORAGE ADDRESS OF DISPLAY PLANE 0 (ADR7n)
243
READ ADDRESS
242B
BUFFER CONTROL UNIT
242A
PIXEL DATA BUFFER
TO THE MEMORY CONTROL UNIT
241
DISPLAY SYNTHESIZING UNIT
5
DISPLAY DEVICE
245
ADR00
ADR01
ADR0n
ADR70
ADR71
ADR7n
D0=0
D0=1
D7=0
D7=1
SELECTION SIGNAL GENERATION STATE MACHINE OF DISPLAY PLANE 0
SELECTION SIGNAL GENERATION STATE MACHINE OF DISPLAY PLANE 7

FIG. 6

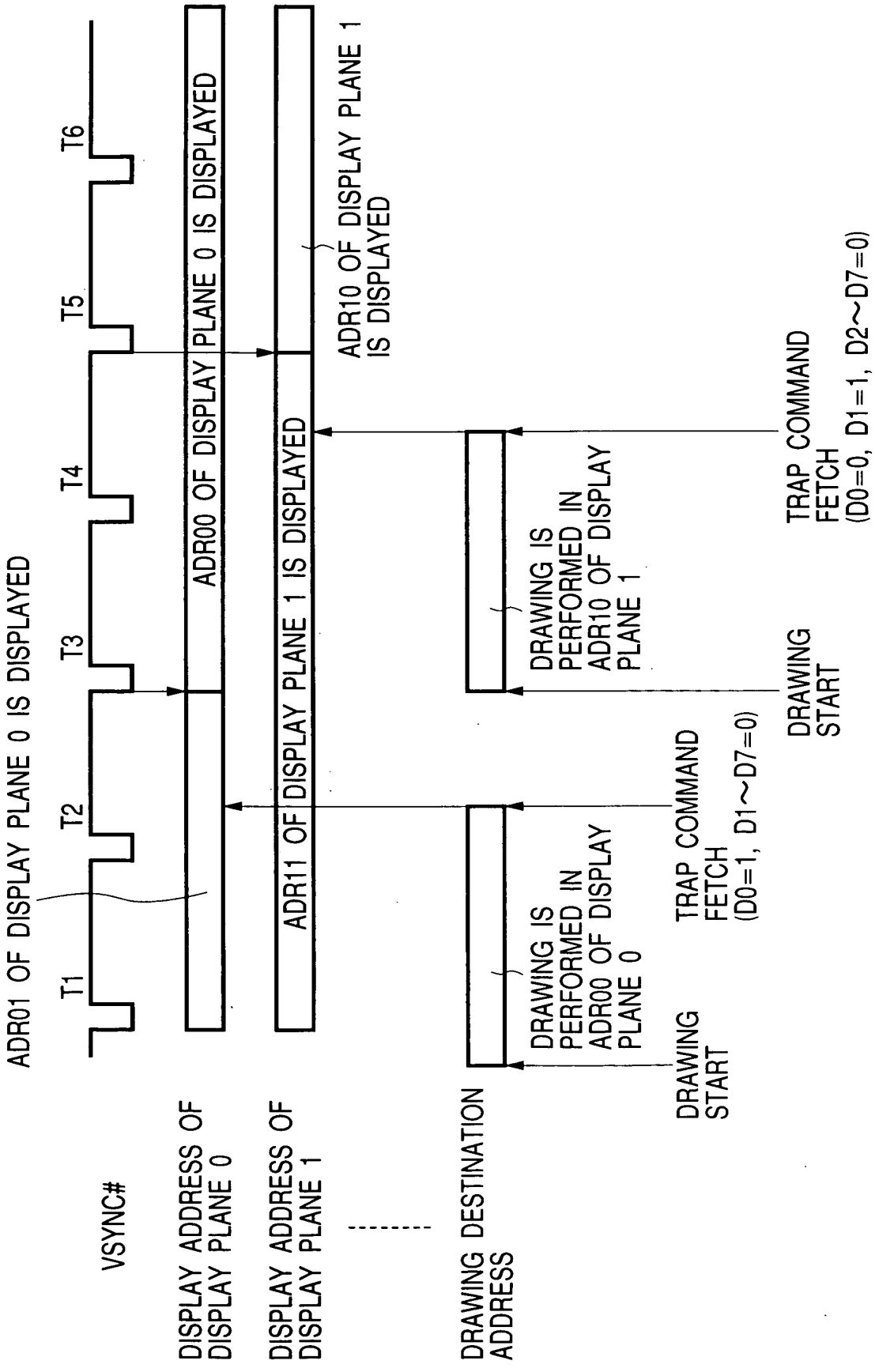

VSYNC#
T1
T2
T3
T4
T5
T6
ADR01 OF DISPLAY PLANE 0 IS DISPLAYED
DISPLAY ADDRESS OF DISPLAY PLANE 0
ADR00 OF DISPLAY PLANE 0 IS DISPLAYED
DISPLAY ADDRESS OF DISPLAY PLANE 1
ADR11 OF DISPLAY PLANE 1 IS DISPLAYED
ADR10 OF DISPLAY PLANE 1 IS DISPLAYED
DRAWING DESTINATION ADDRESS
DRAWING IS PERFORMED IN ADR00 OF DISPLAY PLANE 0
DRAWING IS PERFORMED IN ADR10 OF DISPLAY PLANE 1
DRAWING START
TRAP COMMAND FETCH (D0=1, D1~D7=0)
DRAWING START
TRAP COMMAND FETCH (D0=0, D1=1, D2~D7=0)

FIG. 7

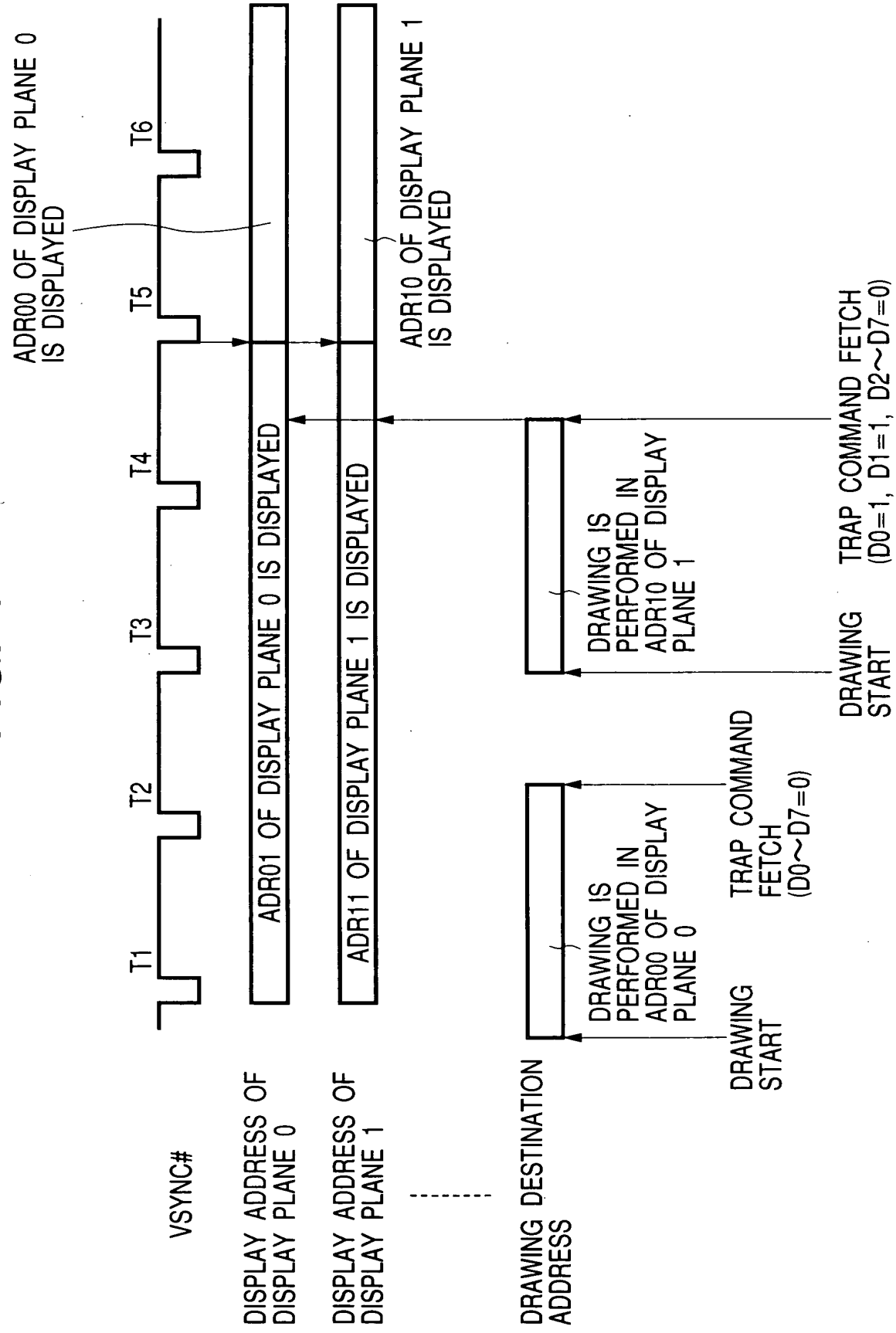

VSYNC#
T1
T2
T3
T4
T5
T6
DISPLAY ADDRESS OF DISPLAY PLANE 0
ADR00 OF DISPLAY PLANE 0 IS DISPLAYED
ADR01 OF DISPLAY PLANE 0 IS DISPLAYED
DISPLAY ADDRESS OF DISPLAY PLANE 1
ADR10 OF DISPLAY PLANE 1 IS DISPLAYED
ADR11 OF DISPLAY PLANE 1 IS DISPLAYED
DRAWING DESTINATION ADDRESS
DRAWING START
DRAWING IS PERFORMED IN ADR00 OF DISPLAY PLANE 0
TRAP COMMAND FETCH (D0~D7=0)
DRAWING START
DRAWING IS PERFORMED IN ADR10 OF DISPLAY PLANE 1
TRAP COMMAND FETCH (D0=1, D1=1, D2~D7=0)

FIG. 8

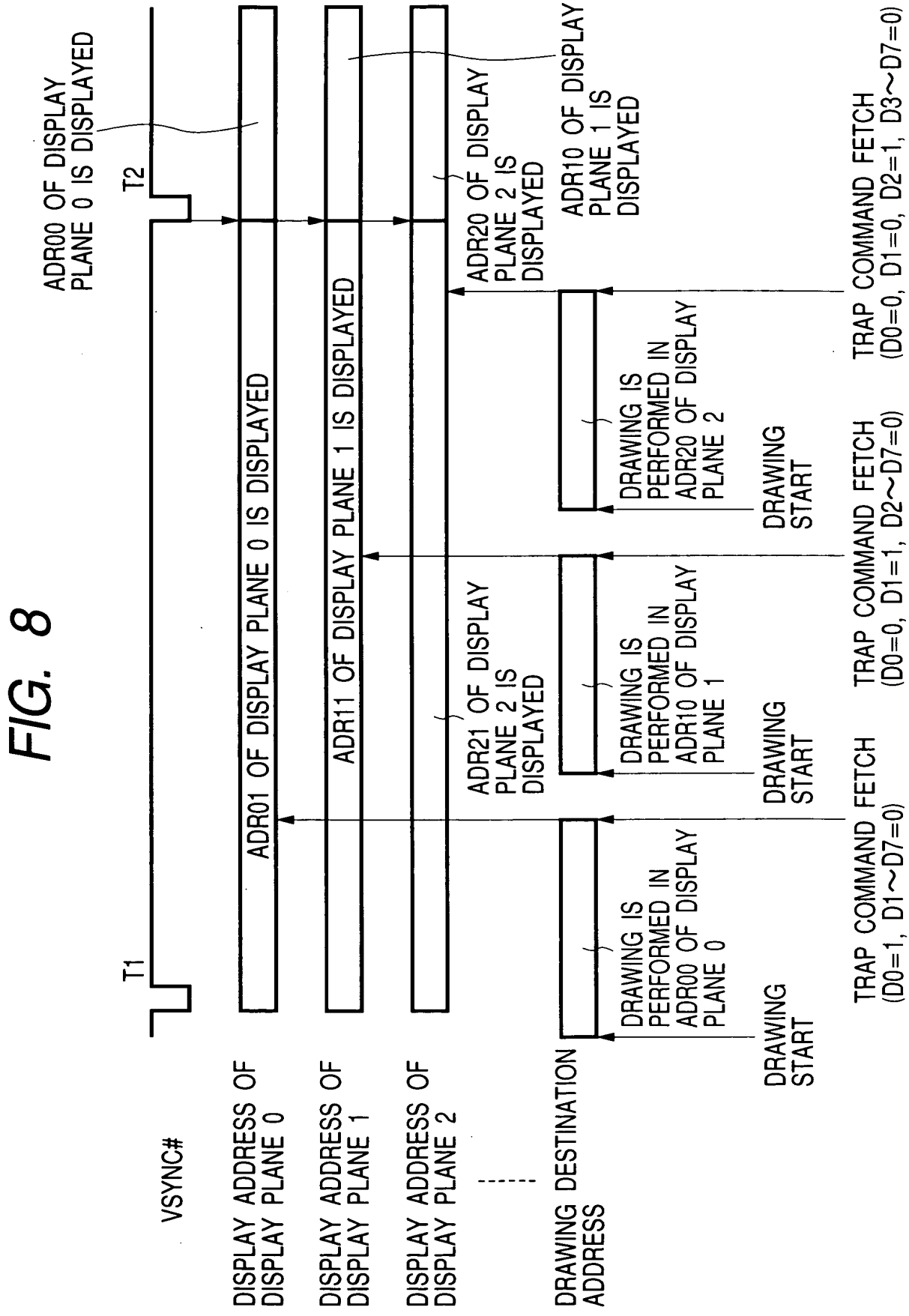
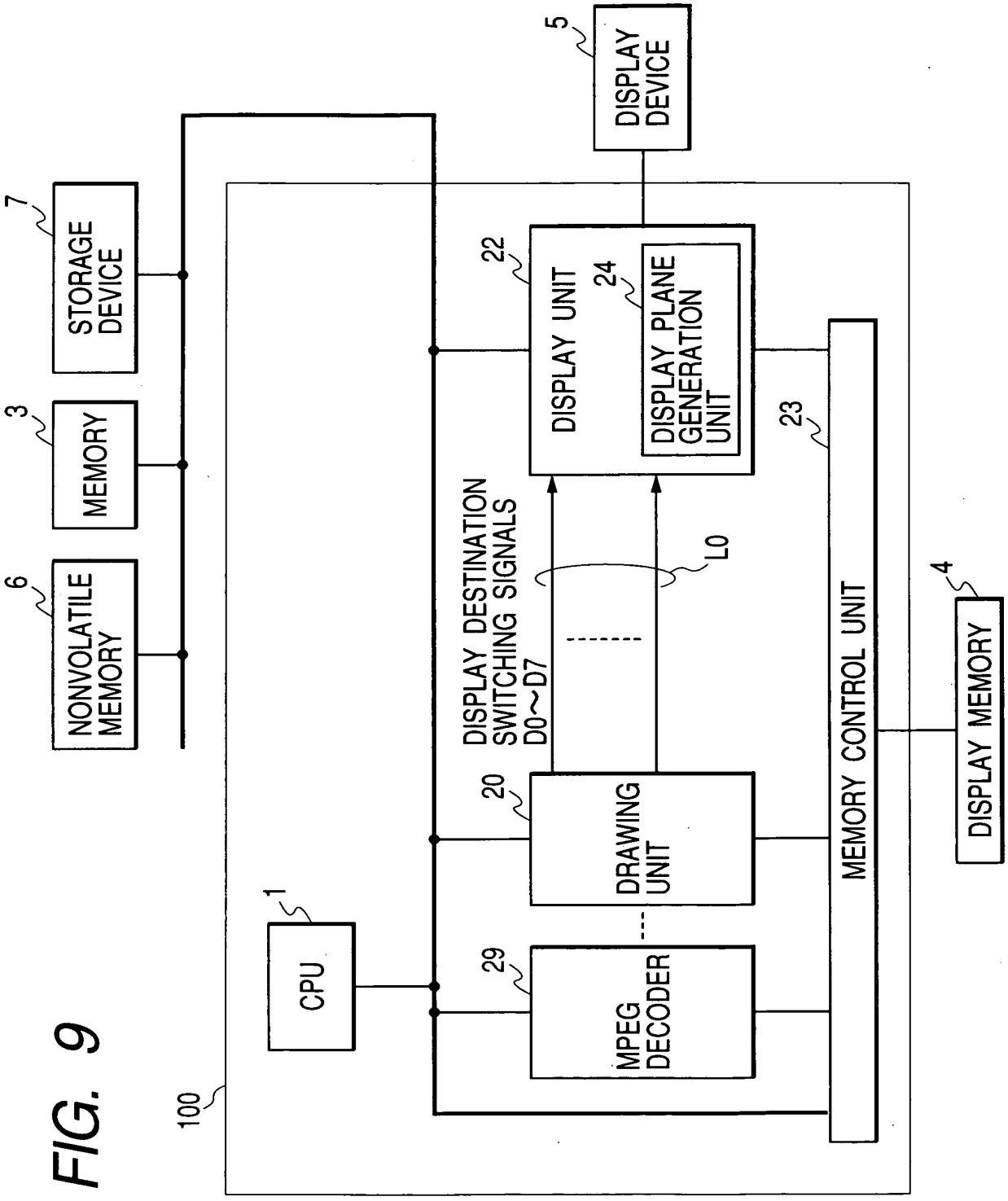

VSYNC#
T1
T2
DISPLAY ADDRESS OF DISPLAY PLANE 0
DISPLAY ADDRESS OF DISPLAY PLANE 1
DISPLAY ADDRESS OF DISPLAY PLANE 2
DRAWING DESTINATION ADDRESS
ADR00 OF DISPLAY PLANE 0 IS DISPLAYED
ADR01 OF DISPLAY PLANE 0 IS DISPLAYED
ADR11 OF DISPLAY PLANE 1 IS DISPLAYED
ADR21 OF DISPLAY PLANE 2 IS DISPLAYED
ADR20 OF DISPLAY PLANE 2 IS DISPLAYED
ADR10 OF DISPLAY PLANE 1 IS DISPLAYED
DRAWING IS PERFORMED IN ADR00 OF DISPLAY PLANE 0
DRAWING IS PERFORMED IN ADR10 OF DISPLAY PLANE 1
DRAWING IS PERFORMED IN ADR20 OF DISPLAY PLANE 2
DRAWING START
DRAWING START
DRAWING START
TRAP COMMAND FETCH (D0=1, D1~D7=0)
TRAP COMMAND FETCH (D0=0, D1=1, D2~D7=0)
TRAP COMMAND FETCH (D0=0, D1=0, D2=1, D3~D7=0)

FIG. 9


100
CPU
1
MPEG DECODER
29
DRAWING UNIT
20
DISPLAY DESTINATION SWITCHING SIGNALS D0~D7
L0
DISPLAY UNIT
22
DISPLAY PLANE GENERATION UNIT
24
MEMORY CONTROL UNIT
23
DISPLAY MEMORY
4
DISPLAY DEVICE
5
STORAGE DEVICE
7
MEMORY
3
NONVOLATILE MEMORY
6